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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/330,231	06/10/1999	ROBERTO PASSERONE	3964-US	9152

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EXAMINER
KING, JUSTIN

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 11/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/330,231	PASSERONE ET AL.	
	Examiner	Art Unit	
	Justin I. King	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The specification is objected. The specification, page 27 lines 1-2, states "a finite state machine rather than a finite automaton is created". The finite automaton is the finite state automaton, and the National Institute of Standards and Technology (NIST) has concluded that the finite state automaton is the finite state machine (http://www.nist.gov/dads/html/finiteStateMachine.html). Applicant's statement has conflicted with the NIST's definition.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9 and 11-20 are rejected under 35 U.S.C. 102(b) as being anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols (application's specification pages 4-5).

Referring to claim 1: Synthesizing Converters Between Finite State Protocols discloses two finite state machines and a third finite state machine for the valid data transfer (specification page 5, lines 3-4). The finite state machine (FSM, also known as automaton) has been long used for data processing simulation, and it is a common and inherited practice to generate a FSM

based a set of given inputs or regular expressions. Hence, it is said that J. Akella and K. McMillan's computer design includes a mean for receiving a first representation/protocol with regular expressions and a mean for receiving a second representation/protocol with regular expressions, and J. Akella and K. McMillan's computer design also includes a mean to generate a finite automaton for each representation.

The topic of the Synthesizing Converters Between Finite State Protocols and the third FSM's given description have explicitly directed Akella and McMillan's computer design to a communication establishment between two FSMs. The specification (page 5, lines 3-4) explicitly discloses that the third FSM represents the valid data transfer; such that it is said the third FSM represents one or more permitted operations of said first and second FSMs.

The Akella and McMillan's computer design creates a product machine, which is pruned of invalid/useless states (specification, page 5, line 5). Since the third FSM only represents the valid data operations between the two protocols, and each protocol's invalid operations or un-convertible operations become non-deterministic (invalid/useless), in order to be pruned of invalid/useless states, it is necessary and obvious to eliminate these non-determinisms either before or after they enter the third FSM. Therefore, it is said applicant's invention is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols.

Referring to claim 2: Claim 2 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated above; furthermore, a FSM is inherent to automatically corresponding data. Upon receiving data, FSM will proceed with appropriate transition and to the next appropriate state.

Referring to claim 3: Claim 3 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated above; furthermore, it is inherent that two different protocols have different data formats and data handling sequences, and the converter is only needed among different protocols.

Referring to claim 4: Claim 4 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated above; furthermore, the initial state's identification, first sequence's identification, regular expression's derivative's constructions, and equivalent expressions' eliminations are the fundamental and basic steps for building a FSM.

Referring to claim 5: Claim 5 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated above; furthermore, collecting and integrating data are the fundamental and basic steps for data analysis.

Referring to claim 6: Claim 6 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated in claim 3 above.

Referring to claim 7: Claim 7 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated in claim 3 above.

Referring to claim 8: Claim 8 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated above; furthermore, it is inherited and obvious that either every states or a selected states from two FSMs will interface via the third FSM. Each FSM remains their own independent operations and each FSM may receive and transmits data to each other via the third FSM. The only communication is either receiving data

or transmitting data; and since the third FSM functions as the converter, it is said the third FSM's states will be their new states to convert data into the opposing protocol's standard. These are fundamental and basic steps for establishing converters among different protocols/FSMs.

Referring to claim 9: Claim 9 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated above; furthermore, the third FSM represents the valid data transfers (specification, page 5, line 4), and in order for any data transfer to be valid, it cannot result in a data inconsistency.

Referring to claim 11: Claim 11 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated claim 4 above.

Referring to claim 12: Claim 12 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated above; furthermore, the storage device and processor are inherent in every computer design. Each protocol needs to transmit its own data to processor to be processed, and this inherited mean for transmitting is equivalent to the receiving unit. The mean for generating the first, second, and third FSMs is equivalent to the automata unit and product unit. The mean for eliminating any non-determinism is equivalent to the determinism unit.

Referring to claim 13: Claim 13 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated claims 2 and 12 above.

Referring to claim 14: Claim 14 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated above; furthermore, the third

FSM's inherited converting function between different protocols is equivalent to the translation unit.

Referring to claim 15: Claim 15 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated claim 4 above.

Referring to claim 16: Claim 16 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated claim 5 above.

Referring to claim 17: Claim 17 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated claim 14 above.

Referring to claim 18: Claim 18 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated claim 8 above.

Referring to claim 19: Claim 19 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated claim 9 above.

Referring to claim 20: Claim 20 is anticipated by J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols as stated claim 1 above; furthermore, the Akella and McMillan's computer design is meant to implemented on a computer system, and it is inherent for every computer system to employ a tangible read medium to perform any program.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols.

The disclosures of J. Akella and K. McMillan's Synthesizing Converters Between Finite State Protocols are discussed in the 102 rejections stated above, and the identifying the non-deterministic transition is a common practice in FSM's construction. It is an inherited practice to select a single outgoing transition for each state's each input.

However, the given information on J. Akella and K. McMillan does not explicitly mention the priority parameters. An "Official Notice" is taken on the following: It is a commonly well-known practice to one in the computer art to incorporate the priority into any computer design.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time applicant made the invention to adapt the priority consideration into J. Akella and K. McMillan because it enables the system to better handle the time-sensitive tasks.

Conclusion

7. The prior art made of recorded and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,845,107 to Fisch et al.: Fisch discloses a signal conversion between two different protocols.

U.S. Patent No. 6,308,147 to Keaveny, Thomas A.: Keaveny teaches that it is known to have the finite state machine dynamically translating address and manipulating the bus control primitives outside of the address phase.

U.S. Patent No. 5,663,666 to Chun et al.: Chu discloses a finite state machine connected to mixed means and a frequency synthesizer, and the finite state machine interprets the mixed signals and generates action commands.

U.S. Patent No. 6,223,274 to Catthoor et al.: Catthoor teaches that it is known to reuse the IP block.

Young, James Shin, Synchronization of Java Threads Using Rendezvous, 1997, http://www-cad.eecs.berkeley.edu/~jimy/java/rendezvous: Young discloses that it is known to identify the non-deterministic states by analyzing all events in a thread effecting the other treads' event behavior, and Young teaches one to impose an order on all such interacting events to eliminate the non-determinism.

Cohen, Daniel I.A., Introduction to Computer Theory, 1997, John Wiley & Sons, 2nd Edition, chapter 6: Cohen teaches one to crate an absorbing non-accepting state.

Bumble, Marc, and Coraor, Lee, Architecture for a Non-Deterministic Simulation Machine, 1998, Computer Science and Engineering, The Pennsylvania State University, page 1600: Bumble and Coraor teach one to eliminate impotent events by splitting event queues.

Chapman, Matt , The Finite State Machine Explorer, 1996, http://www.belgarath.demon.co.uk/java/fsme.html: Chapman discloses his academic software implementation of the FSM from University of Warwick, England.

T. Funkhouser, COS 126 lecture: Formal Languages, spring 1999, http://www.cs.princeton.edu/courses/archive/spr99/cs126/comments/16homsky.html: Funkhouser's computer science 126 class teaches students to eliminate non-deterministic states.

National Institute of Standards and Technology (NIST), http://www.nist.gov/: the NIST's web site provides the definitions for finite state machine, automaton, and non-deterministic finite state machine.

Network Innovation Laboratories, Register Transfer Level Design, 1998, http://www.onlab.ntt.co.jp/member/imlig/sem98/tuthtm/node6.htm: the article illustrates the register transfer level design.

H.H. Ehrenburg and H.A.N. van Maanen, A finite automaton learning system using genetic programming, 1994, CWI Centrum Voor Wiskunde en Informatica Report Rapport: the article discloses the automatically self-learning FSM.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin King whose telephone number is (703) 305-4571. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:00 P.M..

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose number is (703)-306-5631.

Justin King
November 4, 2002

XUAN M. THAI
PRIMARY EXAMINER
TC2100